WHAT IS CLAIMED IS:

1. An integrated circuit chip packaging process comprising the steps of:

(a) preparing a ceramic substrate having a top side on which a plurality of sub-substrates are provided, said sub-substrates each having a die mounting zone and a plurality of pads around said die mounting zone, and then attaching a respective die on the die mounting zone of each said sub-substrate;

(b) electrically connecting the dies at said sub-substrates to said pads;

(c) preparing a mold comprised of a first die and a second die, and then putting the die-attached ceramic substrate thus obtained from said step (a) and step (b) in a cavity of the first die of said mold, and then closing the second die of said mold on said first die by the way of not contacting said second die of said mold to said die-attached ceramic substrate to form an enclosed mold cavity in said mold, and then filling a molten encapsulating material into said enclosed mold cavity to form a molding with a predetermined height on the top side of said ceramic substrate, thereby encapsulating said sub-substrates and the die at each said sub-substrate; and

(d) opening said mold and taking out the encapsulated die-attached ceramic substrate thus obtained from said step (c), and then cutting the encapsulated die ceramic substrate to singulate said sub-substrates into individual.

2. The integrated circuit chip packaging process as claimed in claim 1, further comprising the sub-step of putting an intermediate mold plate in between said first die and said second die during said step (c) before filling a molten encapsulating material into said enclosed mold cavity.

3. The integrated circuit chip packaging process as claimed in claim 1, wherein the size of the cavity of said second die is smaller than the cavity of said first die.